𝒯ℱ𝒰𝒮 2152

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Laurence B. Boucher et al.		Ser. No:	09/692,561
Filing Date:	October 18, 2000	Examiner:	Maung, Z.
Atty. Docket No:	ALA-002A	GAU:	2152

For:　　INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD
　　　　 FOR ACCELERATED PROTOCOL PROCESSING

February 24, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

<center>7th Supplemental Information Disclosure Statement</center>

Sir:

　　Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicants bring sixteen documents to the Examiner's attention. Included are copies of nine non-patent reference documents, and a one-page form PTO-1449 listing these documents separately from seven U.S. Patent reference documents. Copies of the seven U.S. Patent reference documents are not enclosed.
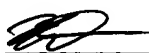
　　Citation of these documents shall not be construed as an admission that the documents are prior art with respect to the instant invention, a representation that a search has been made, or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

Respectfully submitted,

Mark Lauer
Reg. No. 36,578
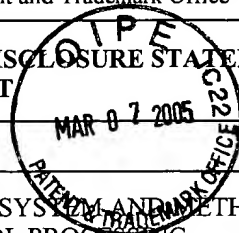6601 Koll Center Parkway
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U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/692,561
7th SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing date: October 18, 2000
	Inventors: Laurence B. Boucher et al.
	Group Art Unit: 2152
INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING	Examiner name: Zarni Maung
	Attorney Docket No. ALA-002A

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A	5,524,250	6/4/96	Chesson et al.	395	775	
	B	5,619,650	4/8/97	Bach et al.	395	200.01	
	C	5,727,142	3/10/98	Chen	395	181	
	D	5,802,258	9/1/98	Chen	395	182.08	
	E	5,898,713	4/27/99	Melzer et al.	371	53	
	F	6,021,507	2/1/00	Chen	714	2	
	G	6,047,323	4/4/00	Krause	709	227	
	H						

OTHER ART—NON PATENT LITERATURE DOCUMENTS

*Examiner Initial	Cite No.	(Including Author, Title, Date, Pertinent Pages, Etc.)
	1	Schwaderer et al., IEEE Computer Society Press publication entitled, "XTP in VLSI Protocol Decomposition for ASIC Implementation", from 15th Conference on Local Computer Networks, 5 pages, Sept. 30 – Oct. 3, 1990.
	2	Beach, Bob, IEEE Computer Society Press publication entitled, "UltraNet: An Architecture for Gigabit Networking", from 15th Conference on Local Computer Networks, 18 pages, Sept. 30 – Oct. 3, 1990.
	3	Chesson et al., IEEE Syposium Record entitled, "The Protocol Engine Chipset", from Hot Chips III, 16 pages, Aug. 26-27, 1991.
	4	Maclean et al., IEEE Global Telecommunications Conference, Globecom '91, presentation entitled, "An Outboard Processor for High Performance Implementation of Transport Layer Protocols", 7 pages, Dec. 2-5, 1991.
	5	Ross et al., IEEE article entitled "FX1000: A high performance single chip Gigabit Ethernet NIC", from Compcon '97 Proceedings, 7 pages, Feb. 23-26, 1997.
	6	Strayer et al., "Ch. 9: The Protocol Engine" from XTP: The Transfer Protocol, 12 pages, July 1992.
	7	Publication entitled "Protocol Engine Handbook", 44 pages, Oct. 1990.
	8	Koufopavlou et al., IEEE Global Telecommunications Conference, Globecom '92, presentation entitled, "Parallel TCP for High Performance Communication Subsystems", 7 pages, Dec. 6-9, 1992.
	9	Lilienkamp et al., Publication entitled "Proposed Host-Front End Protocol", 56 pages, Dec. 1984.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.